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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/921,150	08/02/2001	Jin Chuan Bai	MM4460	7226

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ANDERSON KILL & OLICK P.C.
1251 AVENUE OF THE AMERICAS
NEW YORK, NY 10020-1182

EXAMINER
ZARNEKE, DAVID A

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 07/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/921,150	Applicant(s) BAI, JIN CHUAN	
	Examiner David A. Zarneke	Art Unit 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-8 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8 is/are rejected.

7)☒ Claim(s) 1 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 02 August 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Taiwan on 6/7/01. It is noted, however, that applicant has not filed a certified copy of the Taiwan application as required by 35 U.S.C. 119(b).

Claim Objections

Claim 1 is objected to because of the following informalities: in step 6, line 2, after "connected", the word "to" should be inserted. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al., US Patent 6,333,206, in view of Applicant's admitted prior art and Chen et al., US Patent 6,2620,264, or Nguyen et al., US Patent 6,245,595, or Wang et al., US Patent 6,168,972, or Urushima, US Patent Application Publication 2001/0036711.

Ito teaches a process of producing a semiconductor device comprising:

1) providing a printed circuit board (PCB) substrate (1) having a chip mounting area;

2) disposing a plurality of spherical connecting electrode portions (2) on the chip mounting area and electrically connected to the substrate;

3) depositing an underfill resin layer (13) on the surface of the PCB such that the tops of the connecting electrode portions are exposed; and

4) mounting a semiconductor element (3) such that the electrode portions of the semiconductor element are electrically connected to the exposed ends of the PCB electrode portions (2) (Figures 6 &7 and 10, 40+).

Ito fails to teach the 5th and 6th steps of the claim, namely the encapsulating of the chip and then the implantation of solder balls on the 2nd surface of the substrate.

The examiner takes "official notice" since the claimed subject matter is notoriously well-known in the art (MPEP 2144.03) as evinced by Applicant's admitted prior art which teaches that it is well known in the art to encapsulate the chip after its attachment to the substrate and also to implant solder balls onto the opposite surface of the substrate (Specification, page 1, 3rd paragraph).

Ito also fails to teach conductive electrode portions having a flat end.

The examiner takes "official notice" since the claimed subject matter is notoriously well-known in the art (MPEP 2144.03) as evinced by Chen, Nguyen, Wang and Urushima (see Figures). All of these references teach that flat surfaced solder balls are commonly well known in the art to connect a chip to a substrate.

Regarding claims 2 and 3, Ito teaches the connecting electrode portions as being an eutectic solder bump (5, 29+). Eutectic solder is an alloy of tin and lead.

With respect to claim 4, Chen (7, 11+), Wang (7, 17+) and Urushima (1, [0010]) all teach that it is well known in the art to use CMP or any other etch back process to planarize the encapsulant with the top of the solder bumps.

As to claim 5, Ito teaches that the connecting electrode portions are connected to the bond pads of the substrate, which are electrically connected to the substrate (5, 9+).

Regarding claim 6, Urushima teaches the 2nd encapsulant as encapsulating the entire chip, wherein the 2nd surface of the chip has no bond pads (Figure 5(a)).

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al., US Patent 6,333,206, in view of Applicant's admitted prior art and Chen et al., US Patent 6,2620,264, or Nguyen et al., US Patent 6,245,595, or Wang et al., US Patent 6,168,972, or Urushima, US Patent Application Publication 2001/0036711, as applied to claim 1 above, and further in view of Cook et al., US Patent 6,331,446.

Ito, Applicant's admitted prior art and Chen or Nguyen or Wang or Urushima, all fail to teach the 2nd encapsulant exposing the 2nd surface of the chip, wherein the 2nd surface of the chip has no bond pads.

Cook teaches electrically connecting a chip (18) to a substrate (12) using solder balls (20), depositing a 1st underfill material (24) between the chip and the substrate, and then depositing a 2nd underfill material (26), wherein the 2nd underfill material forms a fillet around the edge of the chip to therefore expose the top surface of the chip.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the fillet 2nd underfill material of Cook in the combined inventions of Ito, Applicant's admitted prior art, and Chen or Nguyen or Wang or Urushima because Cook teaches the 2nd underfill material creates a circumferentic fillet that surrounds and seals the edges of the chip and the 1st underfill to inhibit moisture migration, and cracking of the chip and the 1st underfill material (2, 56+).

Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al., US Patent 6,333,206, in view of Applicant's admitted prior art and Chen et al., US Patent 6,2620,264, or Nguyen et al., US Patent 6,245,595, or Wang et al., US Patent 6,168,972, or Urushima, US Patent Application Publication 2001/0036711, as applied to claim 1 above, and further in view of Lai et al., US Patent 6,323,066.

Ito, Applicant's admitted prior art and Chen or Nguyen or Wang or Urushima, all fail to teach the attachment of a heat sink to the surface of the substrate after the mounting of the chip and its subsequent encapsulation by the 2nd encapsulant.

Lai teaches a prior art heat-dissipating structure comprising attaching a chip to a substrate, attaching a heat sink to the substrate and over the top of the chip, and then encapsulating the heat sink and the chip (Figure 6).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the heat sink of Lai in the combined inventions of Ito, Applicant's admitted prior art, and Chen or Nguyen or Wang or Urushima because Lai teaches this type of heat sink attachment prevents resin flow during the molding process and also

prevents the heat sink from causing a thermal compressive stress in the chip during the cooling process (2, 30+).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Brand, US Patent Application Publication 2002/0019075, and Milkovich et al, US Patent 6,100,114, both are cited as teaching the state of the art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (703)-305-3926. The examiner can normally be reached on M-Th (7:30-6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703)-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703)-308-7722 for regular communications and (703)-308-7721 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-308-0956.

David A. Zarneke
June 28, 2002